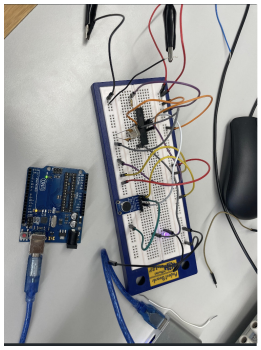
ZIQIN (GARRY) YUAN

Electrical Engineering Student | University of New South Wales

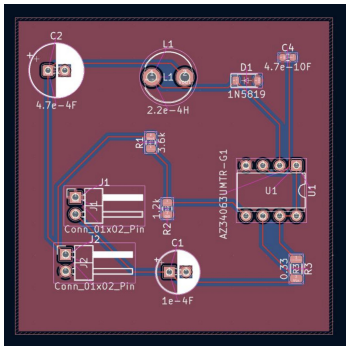
garryyuan1@gmail.com | +61 451 961 015 | Sydney, Australia | Australian Citizen

This portfolio presents selected hardware engineering projects built during my undergraduate studies in Electrical Engineering at UNSW. Every project was physically constructed, simulated in LTSpice or MATLAB, and validated on the bench. Tools: KiCAD (PCB design), LTSpice (circuit simulation), MATLAB (signal processing), C/C++ (embedded firmware).

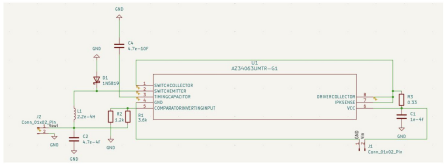
Project 1 — Touchless Gesture-Controlled Light Switch



Assembled breadboard — Arduino Uno, IR sensor, MAX9814 mic module



KiCAD PCB layout — AZ34063U buck converter, 2-layer FR-4



Schematic Circuit Diagram

LTSpice schematic — buck converter circuit

What?

- A contactless light switch activated by hand gesture or clap
- Reduces wear and physical contact in shared spaces
- Fully self-contained: 9V battery powered

How?

Sharp GP2Y0D810Z0F IR sensor, 2-10 cm range

MAX9814 microphone for clap activation

ATmega328P C++ firmware — debounce, relay control

AZ34063U KiCAD PCB buck converter (9V → 5V)

LTSpice simulation before build

Result?

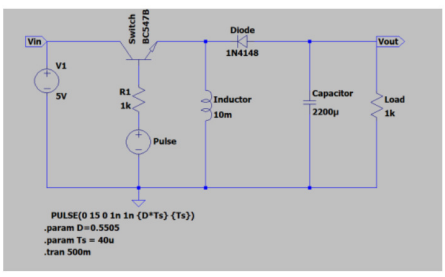
↓ **60%** false trigger reduction

3-9.5 cm adjustable detection range (trimpot)

ERC/DRC clean KiCAD PCB, BOM generated

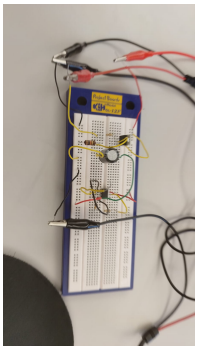
Self-contained no bench supply required

Project 2 — LM741 Negative Power Supply (Inverting Buck-Boost Converter)



LTSpice schematic — 555 timer PWM, N-MOSFET, flyback diode, 2200 µF cap

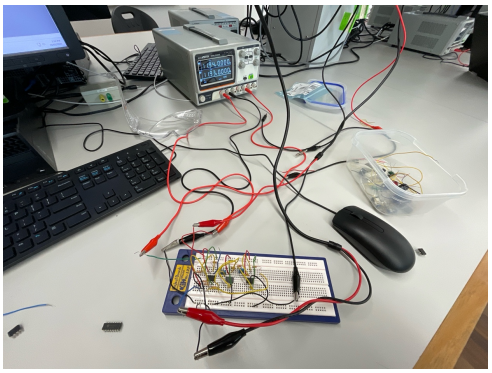
Oscilloscope — stable -5.0V rail, ripple below 320 mV



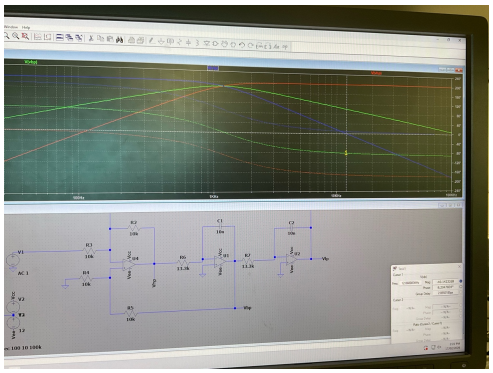
Breadboard under 100 Ω to 100 kΩ resistive load

What?	How?	Result?
• Generate a stable -5V rail from a single positive supply • Enable dual-rail LM741 op-amp operation • Self-contained: no external signal generator needed	**Inverting buck-boost** N-MOSFET + 1 mH inductor + 1N4148 diode **555 timer** ~25 kHz self-contained PWM clock **2200 µF** output capacitor for ripple smoothing **LTSpice** full transient simulation before build	**-5.0V** stable output under 50 mA load **<320 mV** output ripple **6.3V p-p** sine wave from powered LM741 **First build** met spec — no rework needed

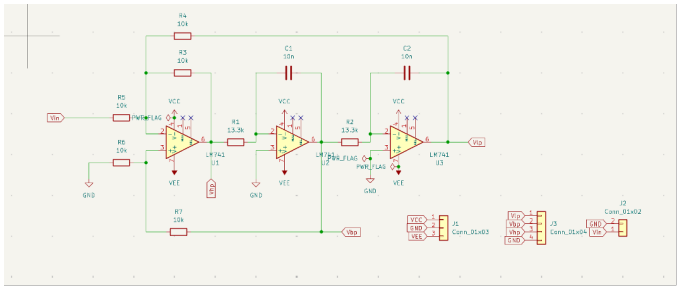
Project 3 — Analog Filtering Circuit (LP / HP / BP Active Filter)



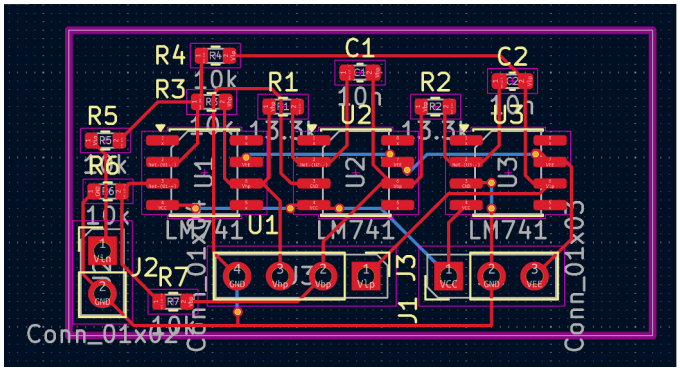
Breadboard — LM741 filter under ±12V bench supply, three outputs probed



LTSpice AC Bode plot — LP (blue), BP (green), HP (orange) at f■ = 1.2 kHz



KiCAD schematic — U1 input buffer, U2 MFB bandpass, U3 LP output buffer



KiCAD PCB — 3× LM741 (DIP-8), GND pour on B.Cu, 0 signal vias

What?

- Single-input, 3-output active filter: LP + HP + BP simultaneously
- Cutoff frequency 1.2 kHz from ±12V supply
- Meet 4 simultaneous hard specifications

How?

2nd-order active LP/HP topology → 40 dB/decade rolloff

MFB topology bandpass — independent f■, Q, gain control

Unity-gain buffers on all 3 outputs → ≤1 kΩ output impedance

R = 10 kΩ, C = 10 nF standard values, tolerance-robust

KiCAD PCB schematic + ERC + layout + DRC

Result?

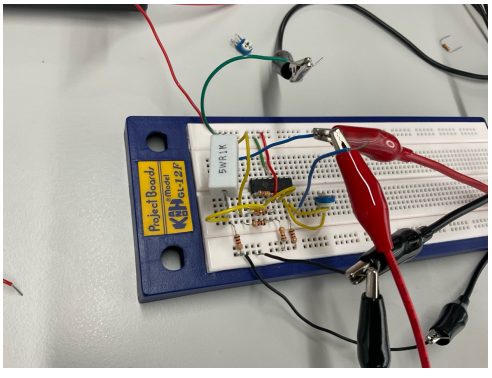
1.2 kHz cutoff confirmed on oscilloscope

>40 dB/decade rolloff (spec: 35 dB)

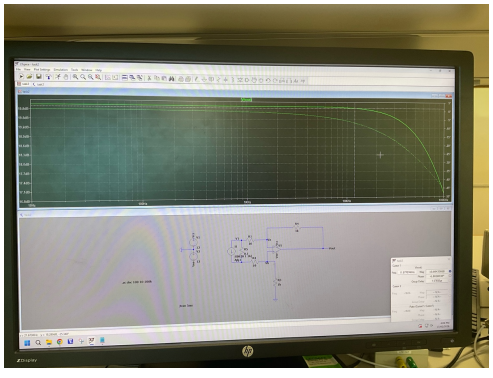
±1.5 dB passband ripple — spec met

ERC/DRC clean ~90×55 mm 2-layer PCB

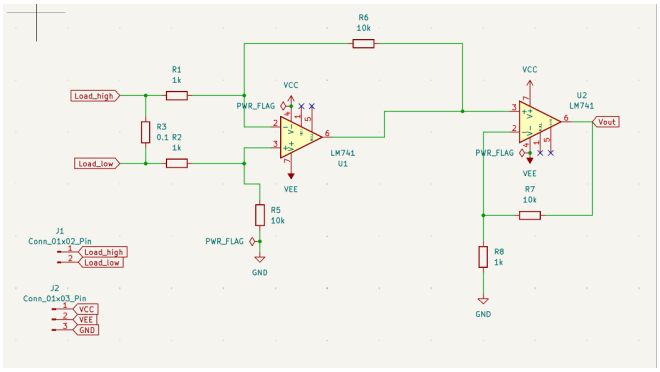
Project 4 — Current Measurement Amplifier (Variable Gain, G = 10-100)



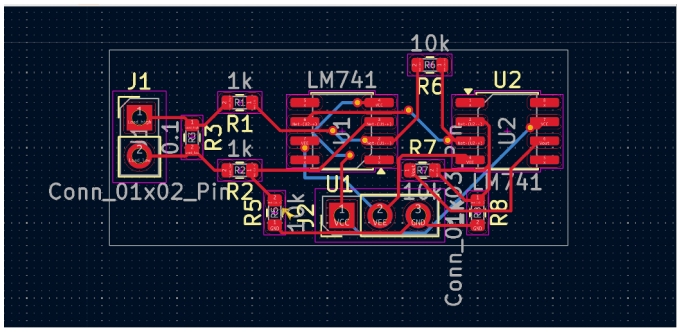
Breadboard — 5WR1K shunt (white), LM741, trimpot gain control



LTSpice AC response — flat within ±3 dB from 100 Hz to 12 kHz at G = 100



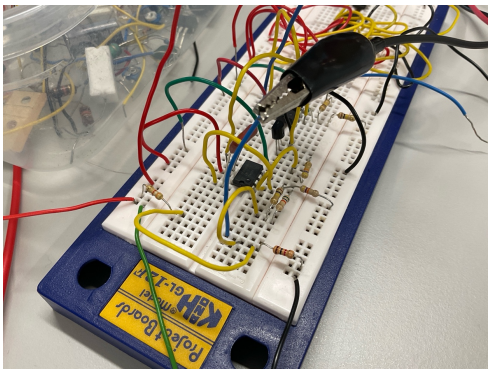
KiCAD schematic — 3-op-amp instrumentation amp, 0.1 Ω shunt, output buffer



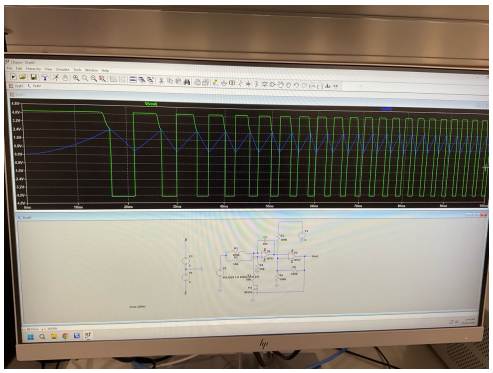
KiCAD PCB — shunt adjacent to J1, trimpot on board edge, GND pour

What?	How?	Result?
• Current-to-voltage amplifier, G = 10-100 (continuous) • Works high-side or low-side — no rewiring • Flat response 100 Hz to 10 kHz	**0.1 Ω shunt** 100 mV drop at 1A full scale, 100 mW dissipation **3-op-amp IA** rejects common-mode, enables ± placement **Single trimpot** sets G = 10-100 continuously **Output buffer** 1 kΩ series resistor → ≤1 kΩ impedance **KiCAD PCB** shunt placed adjacent to sense connector	**G = 10-100** via trimpot — no component swap **±3 dB** 100 Hz to >10 kHz bandwidth **High + low side** both configurations validated ≤**0.5** Ω parasitic minimised by PCB placement

Project 5 — Voltage-Controlled Oscillator (VCO)



Breadboard — integrator IC (left), Schmitt trigger IC (right), NMOS (centre), trimpots



LTSpice transient — triangle wave (blue) and square wave (green); frequency rises with Vctrl

What?	How?	Result?
• VCO mapping 1V → 1 kHz, 4V → 10 kHz (linear) • Output within 0-5V rail • Dual outputs: triangle wave + square wave	**Integrator core** op-amp + cap ramps linearly; higher Vctrl = faster ramp **Schmitt trigger** comparator with hysteresis defines thresholds **NMOS switch** discharges integrator cap at each threshold crossing **2× 50 kΩ trimpots** independent tuning of frequency range and linearity **LTSpice** transient simulation before bench calibration	**1-10 kHz** output range — spec met **Linear** monotonic mapping confirmed 1-4V **0-5V** both waveforms within supply rail **Stable** no non-linearity or instability observed

Technical Skills

Hardware Design
- Analog circuit design
- Op-amp topologies (LM741, LM324)
- Active filter design (LP/HP/BP)
- Instrumentation amplifiers
- DC-DC power converters

PCB Design
- KiCAD — schematic + ERC
- PCB layout + DRC
- 2-layer FR-4 boards
- GND pour strategy
- Gerber export, BOM

Simulation
- LTSpice — transient, AC, parametric
- MATLAB / Simulink
- ADS (Advanced Design System)
- Simulation-first methodology

Embedded & FPGA
- C / C++ on ATmega328P
- ADC, PWM, GPIO, interrupts
- Sensor interfacing
- Verilog / SystemVerilog / VHDL
- Vivado / Quartus (ELEC2141)

Programming
- C, C++, Python, MATLAB
- MIPS Assembly
- Git version control
- Shell scripting

Field & Test
- LV electrical installation
- Solar/inverter commissioning
- Oscilloscope, bench PSU, DMM
- AS/NZS wiring standards

Ziqin (Garry) Yuan • garryyuan1@gmail.com • +61 451 961 015 • Australian Citizen
BE(Hons) Electrical Engineering / Computer Science | UNSW | 2022-2026

Seaward PAC3760 DL PAT tester — earth bond, insulation resistance & leakage current tests to AS/NZS 3760:2022

What is PAT Testing?

Portable Appliance Testing (PAT) is the systematic electrical safety inspection of in-service equipment to AS/NZS 3760:2022. Every appliance undergoes three sequential measurements:

• **RPE (Earth Resistance) — Ω:** Verifies the low-resistance path between the appliance chassis and earth. A high value indicates a broken earth conductor — dangerous under fault conditions.

• **RISO (Insulation Resistance) — MΩ:** Applies 500 V DC across live-to-earth and neutral-to-earth. Low insulation resistance signals degraded or damaged insulation — a direct shock and fire risk.

• **ILEAK (Leakage Current) — mA:** Measures current flowing from live conductors through insulation to earth under normal operating voltage. Excess leakage triggers RCD tripping and indicates insulation failure.

Equipment

Seaward PAC3760 DL — a professional-grade, data-logging PAT tester with Australian 3-pin socket, onboard RCD test capability (10 mA / 30 mA), 3-phase testing, and USB data download for compliance record generation.

What?

• Perform full PAT testing on electrical appliances across residential and commercial sites
• Conduct visual inspection, earth bond, insulation resistance, and leakage current tests

How?

• **Seaward PAC3760 DL** — earth bond (RPE), insulation resistance (RISO 500 V DC), leakage current (ILEAK)
• **Visual inspection** — checking cable condition, plug integrity, enclosure damage, and correct fusing

Result?

• **AS/NZS 3760:2022 compliant** test and tag records produced for every site
• **Systematic fault detection** — identified and quarantined unsafe appliances before re-energisation
• **Accurate compliance documentation** — test registers and tag records maintained for client audit-readiness

Engineering Relevance

PAT testing applies a rigorous, specification-driven pass/fail methodology to real electrical systems — directly analogous to hardware validation and bench testing in engineering design. Each test sequence mirrors the structured measurement approach used in circuit characterisation: define a parameter, apply a stimulus, measure the response, compare to threshold, and document the outcome.